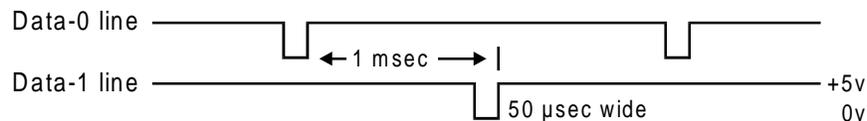


Wiegand Interface Definition

ELECTRICAL CHARACTERISTICS

Wiegand card readers contain a digital buffering circuit in which the signals generated in the read head by the Wiegand wires are separated into discrete digital "1" and "0" data pulses.

Typically the data is buffered and then output on two separate electrical signal lines with a common signal ground line. The data is transmitted at a fixed rate independent of the speed that the card was pulled through the reader. Both data lines are normally held high (typically +5vDC referenced to logic common), and are pulled low (typically TTL logic levels) for the duration of each output pulse. A data "0" is represented by lowering the Data-0 output line while the Data-1 output line remains high. A "1" is represented by lowering the Data-1 output line while the Data-0 output line remains high. A typical pulse width is 50 microseconds with an inter-pulse spacing of 1 millisecond (refer to the diagram below). The actual timing values and tolerances and output circuitry are determined by the card reader manufacturer.

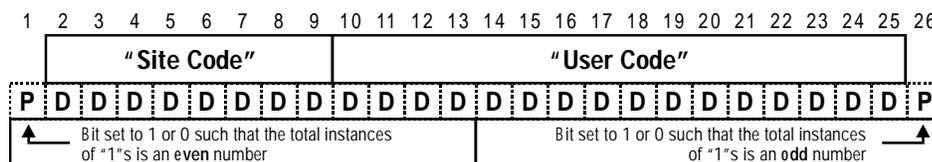


The data packets are separated by a short dwell time (i.e. 500 milliseconds between cards). "Wiegand" proximity tag readers emulate the data stream of a card containing Wiegand wires.

DATA PROTOCOL

There are several different protocols used for transmitting serial data in a "Wiegand" format.

One common format consists of a 26 bit long serial stream consisting of 24 data bits and leading and trailing parity bits. The leading bit in the stream is set to generate an even parity for the first 13 bits transmitted while the trailing bit is set to result in an odd parity for the final 13 bits transmitted. The 24 bits of data is then divided into an 8 bit "site code" followed by a 16 bit "user code" with the most significant bit for each code transmitted first. In the following diagram **P** represents the parity bits and **D** represents the data bits.



Other "Wiegand" formats send different numbers of data bits (ranging from 4 to 44) with different (or no) parity and with possibly some of the bits set high or low at fixed locations in the serial stream. The data itself can be partitioned in to any form imaginable.

Specifications subject to change

TD2058